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"SPI-4" and system-packet-interface

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[CITATION] **System Packet Interface Level 4 (SPI-4) Phase 2: OC-192 System Interface for Physical and Link Layer ...**

R Cam, R Tuck - OPTICAL INTERNETWORKING FORUM, January, 2001

[Cited by 7](#) - [Related articles](#) - [Web Search](#)

Implementation of 10gigabit packet switching using IXP network processors

C Sheng, Z Xu, C Yingxin, D Wei - Communication Technology Proceedings, 2003. ICCT 2003. ..., 2003 - [ieeexplore.ieee.org](#)

... external interfaces: Receive and transmit interfaces, each of which can be individually configured for either the **SPI-4 Phase 2 (System Packet Interface)** to a ...

[Cited by 4](#) - [Related articles](#) - [Web Search](#)

Optical networking module including protocol processing and unified software control

IC Denton, B Murdock, JL Gimlett, EL Hershberg, SW ... - US Patent App. 10/414,115, 2003 - Google Patents
... to Point Protocol SDH Synchronous Digital Hierarchy SONET Synchronous Optical network,
a PHY telecommunication protocol **SPI-4 System Packet Interface Level 4 ...**

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A scalable 10 Gb/s line-rate router with DiffServ support

Y Xu, Z Dai, B Liu, W Li - Communication Technology Proceedings, 2003. ICCT 2003. ..., 2003 - [ieeexplore.ieee.org](#)

... A. Bur Interface Module (BIM) BIM completes the wnvelson between interior data bus and **SPI-4 bus (System Packet Interface Level 4)**, which defines the data ...

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System packet interface

AB Evans, MI Tatar, CK Begin - US Patent App. 10/458,357, 2003 - Google Patents

... board-level interface is the SPI-4.2 **system packet interface** described by the Optical Internetworking Forum in "**System Packet Interface Level 4 (SPI-4) Phase 2 ...**

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Hypertransport/SPI-4 interface supporting configurable deskewing

LR Moll, M Gulati - US Patent App. 10/742,060, 2003 - Google Patents

... 8,2004 (54) HYPERTRANSPORT/**SPI-4** INTERFACE SUPPORTING CONFIGURABLE DESKEWING (76)
Inventors: Laurent R. Moll, Saratoga, CA (US); Manu Gulati, San Francisco, CA ...

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System interface for cell and/or packet transfer at aggregate data rates of up to 10 Gb/s

R Cam, JR Hamstra, W Mok, D Wong - US Patent App. 09/756,680, 2001 - Google Patents

... 4 illustrates the **SPI-4 FIFO status indication**; [0025] FIG. ... 6. POS-PHY Level 4 is the **system packet interface** for data transfer between the link layer and the ...

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Optimized data path structure for multi-channel management information base (MIB) event generation

S Ni - US Patent App. 10/090,845, 2002 - Google Patents

... In a channelized switch system, such as a **SPI-4 (System Packet Interface Level**

4) interface, generating MIB events becomes a nontrivial task. ...

[Web Search](#) - All 5 versions

System having two or more packet interfaces, a switch, a shared packet DMA (Direct Memory Access) ...

BJ Sano, LR Moll, K Oner, M Gulati - EP Patent 1,313,273, 2003 - freepatentsonline.com

... in claim 4 wherein one of the two or more interfaces is a **system packet interface**. ...

level 5). In one particular embodiment, the interfaces may be **SPI-4** phase 2 ...

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System and method for efficient handling of network data

O Uzrad-Nali, S Gupta - US Patent App. 10/014,602, 2001 - Google Patents

... In yet another alternate implementation a **System Packet Interface** Level 3 (SPI-3)

or a System Packet Physical Interface Level 4 (**SPI-4**) may be used. ...

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Method and apparatus for transmission on a 2-bit channel using 3b/4b code

JL Calvignac, JJ Lynch, DJ Sucher, FJ Verplanken - US Patent App. 10/096,161, 2002 - Google Patents

... Details of the **SPI-4** interface is set forth in the OIF document titled: "**System Packet Interface** Level 4 (**SPI-4**) Phase 2: OC-192 System Interface for Physical ...

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Distributed copies of configuration information using token ring

L Moll, JB Rowlands - US Patent App. 10/684,909, 2003 - Google Patents

... j > PCI/PCI-x < » HT/ **SPI-4** 162 mi HT/ **SPI-4** 170 SPI4 ... ISA (industry standard architecture) bus, USB (universal serial bus), and SPI (**system packet interface**). ...

[Web Search](#) - All 4 versions

Message transfer system

A Lines, C Stoops, E Peterson, A Gravel - US Patent App. 10/452,782, 2003 - Google Patents

... interface 108, a JTAG/EJTAG interface 110, a general purpose input/output (GPIO)

interface 112, and a **System Packet Interface** Level 4 (**SPI-4**) Phase 2114. ...

[Web Search](#) - All 2 versions

Robust and scalable de-skew method and apparatus for data path skew control

JM Chiang - EP Patent 1,355,465, 2003 - freepatentsonline.com

... 1. **SPI-4** is the **system packet interface** for data transfer between the link layer and the PHY device; it is designed to meet requirements of this particular ...

[Web Search](#) - All 3 versions

Circuit and method for processing communication packets and valid data bytes

AP Annadurai, F Han, M Rahman, C Tsu - US Patent App. 10/067,226, 2002 - Google Patents

... traffic. The framer communicates with the processor through an inter- face known as the **SPI-4 (system packet interface)**. The **SPI** ...

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Multiple processor integrated circuit having configurable packet-based interfaces

B Sano, L Moll, M Gulati, J Keller - US Patent App. 10/356,390, 2003 - Google Patents

Page 1. US 20040019704A1 (19) United States (12) Patent Application Publication

(io> Pub. NO.: US 2004/0019704 AI Sano et al. (43) Pub. Date: Jan. ...

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Simplifying verification of an SFI converter by data format adjustment

S Goyal, J Parvereshi - US Patent App. 10/373,265, 2003 - Google Patents

... interfaces within a SONET/SDH based communication sys- tem: **system packet interface** ("SPI") 110 and ... interfaces have been defined, such as SPI-3, **SPI-4**, SFI-4 ...

[Web Search](#) - All 4 versions

Method and apparatus for unscheduled flow control in packet form

EG Chen, R Cherukuri, R Wadhawan - US Patent App. 10/021,152, 2001 - Google Patents

... IP packet traffic is the Optical Internetworking Forum **System Packet Interface** Level 4 ... includes a command from the Optical Internetworking Forum **SPI-4** Phase 2 ...

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Data path optimization algorithm

SH NI - US Patent App. 09/982,794, 2001 - Google Patents

... in applications such as aggregating multiple-Gigabit ports to an uplink interface back-plane such as a **System Packet Interface** Level 4 (**SPI-4**) Phase 2 ...

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Fastpath implementation for transparent local area network (LAN) services over multiprotocol label ...

L Shankar, S Ambe - US Patent App. 10/377,664, 2003 - Google Patents

... For example in the embodiment of FIG. 5, the physical port may be an interface such as a **System Packet Interface** Level 4 (**SPI-4**) port channel. ...

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Bandwidth allocation fairness within a processing system of a plurality of processing devices

M Gulati - US Patent App. 10/356,346, 2003 - Google Patents

Page 1. US 20040030799A1 (19) United States (12) Patent Application Publication (io> Pub. NO.: US 2004/0030799 AI Gulati (43) Pub. Date: Feb. ...

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Interconnecting network processors with heterogeneous fabrics

G Leibzay, DW Gish, NC Oliver - US Patent App. 10/313,783, 2002 - Google Patents

... Interface for Physical and Link Layer Devices," dated June 2000 ("SPI-3 Specification"), the OIF document titled "**System Packet Interface** 4 (**SPI-4**) Phase 2: OC ...

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A method and apparatus for solving data burst problems using two buses

NY Chu, JM Chiang - EP Patent 1,345,128, 2003 - freepatentsonline.com

... 1, system 100 may include an interface 103 between an external device 102 and an internal device 105, which may be a **SPI-4 (System Packet Interface** Level 4 ...

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Hypertransport exception detection and processing

JB Rowlands, L Moll - US Patent App. 10/684,953, 2003 - Google Patents

... standard architecture) bus, USB (universal serial bus), and SPI (**system packet interface**). ... 162, 166,170, such as three flexible HyperTrans- port/**SPI-4** Phase 2 ...

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Dynamic resource allocation systems and methods

VK Balakrishnan - US Patent App. 10/719,469, 2003 - Google Patents

... packets to other processor(s) or circuitry connected to the fabric; an interface 105 (eg, a **System Packet Interface** Level 4 (**SPI-4**) interface) that enables ...

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Apparatus and method for header processing

SH NI - EP Patent 1,313,291, 2003 - freepatentsonline.com

... employed in applications such as aggregating multiple-Gigabit ports to an uplink interface backplane such as a **System Packet Interface** Level 4 (**SPI-4**) Phase 2 ...

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Packet data recovery system

GR McLeod - US Patent App. 10/448,008, 2003 - Google Patents

... [0005] As an example, a bus standard that provides such flexibility is the **System Packet Interface** Level 4 Phase 2 (**SPI-4** Phase 2) bus standard specification ...

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Multi-protocol networking processor with data traffic support spanning local, regional and wide

area ...

C Denton, JL Gimlett - US Patent App. 09/860,207, 2001 - Google Patents

... Point to Point Protocol SFD Starting Frame Delimiter SONET Synchronous Optical network, a PHY telecommunication protocol **SPI-4 System Packet Interface** Level 4 ...

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Transmitting data from a plurality of virtual channels via a multiple processor device

M Gulati, L Moll, J Keller - US Patent App. 10/356,348, 2003 - Google Patents

Page 1. US 20040017813A1 (19) United States (12) Patent Application Publication

(io> Pub. NO.: US 2004/0017813 AI Gulati et al. (43) Pub. Date: Jan. ...

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Method and apparatus utilizing a tail bus to solve back-to-back data burst problems

NY Chu, JM Chiang - US Patent App. 10/269,989, 2002 - Google Patents

... 1, system 100 may include an interface 103 between an external device 102 and an internal device 105, which may be a **SPI-4 (System Packet Interface** Level 4 ...

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Smart routing between peers in a point-to-point link based system

M Gulati - US Patent App. 10/421,988, 2003 - Google Patents

Page 1. US 20030217177A1 (19) United States (12) Patent Application Publication

(io> Pub. NO.: US 2003/0217177 AI Gulati (43) Pub. Date: Nov. ...

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Bridges performing remote reads and writes as uncacheable coherent

JB Rowlands - US Patent App. 10/685,136, 2003 - Google Patents

... standard architecture) bus, USB (universal serial bus), and SPI (**system packet interface**). ... 162, 166,170, such as three flexible HyperTransport/**SPI-4** Phase 2 ...

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Apparatus and method to receive and align incoming data in a buffer to expand data width by

...

M Gulati, LR Moll - US Patent App. 10/685,231, 2003 - Google Patents

... Sheet 5 of 7 US 2004/0151203 AI 700 \ **SPI-4** DATA STREAM 8 ... based on certain communicating protocols, such as SPI (**system packet interface**) and hypertransport ...

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Data link/physical layer packet diversion and insertion

DR Primrose, IC Denton - US Patent App. 09/918,691, 2001 - Google Patents

... SDH Synchronous Digital Hierarchy SONET Synchronous Optical network, a PHY telecommunication protocol SOP Start of Packet **SPI-4 System Packet Interface** Level ...

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Distributed 4-bits diagonal interleaved parity (DIP4) checker

NY Chu - US Patent App. 10/234,165, 2002 - Google Patents

... 2 of 15 US 2003/0182613 AI Chip Boundary 110 J r 130 ^ nctrlr?'01 rctl - eg en | 3 rdat[15:0] - 2xrclk rclk PLL ^pi xclk ^125 External 16 bit **SPI-4** data bus ...

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System and method for providing isolated fabric interface in high-speed network switching and

...

SA Sarkinen, JD Swart, NA Schlegel, JM Meyer, DL ... - US Patent App. 09/995,410, 2001 - Google Patents

... Another such standard is the Optical Internetworking Forum (OIF) **System Packet Interface-4 (SPI-4)** which describes a data path interface between the physical ...

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Protocol data unit queues

D Romano, G Wolrich, DF Hooper - US Patent App. 10/460,289, 2003 - Google Patents

... The processor 200 can also feature an interface (eg, a **System Packet Interface** Level 4 (**SPI-4**) interface) that enables to the processor 200 to communicate with ...

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Network statistics

S Jain, DF Hooper - US Patent App. 10/628,997, 2003 - Google Patents

... The processor 200 can also feature an interface 202 (eg, a **System Packet Interface Level 4 (SPI-4)** interface) that enables to the processor 200 to communicate ...

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Data alignment systems and methods

CM Lin - US Patent App. 10/749,328, 2003 - Google Patents

... mitting packets to other processor(s) or circuitry connected to the fabric; an interface 105 (eg, a **System Packet Interface Level 4 (SPI-4)** interface) that ...

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Efficient routing of packet data in a scalable processing resource

B Sano, L Moll, M Gulati - US Patent App. 10/356,323, 2003 - Google Patents

Page 1. US 20040030712A1 (19) United States (12) Patent Application Publication

(io> Pub. NO.: US 2004/0030712 AI Sano et al. (43) Pub. Date: Feb. ...

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Apparatus and method for allocating resources within a security processing architecture using

...

MR Hussain, R Kessler, PH Dickinson - US Patent App. 10/411,943, 2003 - Google Patents

Page 1. US 20040205331A1 (19) United States (12) Patent Application Publication

(io> Pub. NO.: US 2004/0205331 AI Hussain et al. (43) Pub. Date: Oct. ...

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Multi-service queuing method and apparatus that provides exhaustive arbitration, load balancing, and ...

SA Sarkinen, SA Davidson - US Patent App. 09/957,751, 2001 - Google Patents

Page 1. US 20030058880A1 (19) United States (12) Patent Application Publication

(io> Pub. NO.: US 2003/0058880 AI Sarkinen et al. (43) Pub. Date: Mar. ...

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Programmable multi-service queue scheduler

SA Sarkinen, SA Davidson - US Patent App. 09/957,750, 2001 - Google Patents

... to the ingress processing circuit 214 via an interface 216, such as the Optical Internetworking Forum (OIF) **System Packet Interface-4 (SPI-4)**. OIF **SPI-4** ...

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Switch operation scheduling mechanism with concurrent connection and queue scheduling

L Moll - US Patent App. 10/685,376, 2003 - Google Patents

Page 1. US 20040078459A1 (19) United States (12) Patent Application Publication

(io> Pub. NO.: US 2004/0078459 AI Moll (43) Pub. Date: Apr. ...

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Packet data service over hyper transport link (s)

M Gulati, L Moll, B Sano - US Patent App. 10/356,661, 2003 - Google Patents

Page 1. US 20040037313A1 (19) United States (12) Patent Application Publication

(io> Pub. NO.: US 2004/0037313 AI Gulati et al. (43) Pub. Date: Feb. ...

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Apparatus and method for allocating resources within a security processing architecture using

...

MR Hussain, PH Dickinson, I Badr - US Patent App. 10/411,944, 2003 - Google Patents

Page 1. US 20050060558A1 (19) United States (12) Patent Application Publication

(io> Pub. NO.: US 2005/0060558 AI Hussain et al. (43) Pub. Date: Mar. ...

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Centralized switching fabric scheduler supporting simultaneous updates

L Moll, M Gulati - US Patent App. 10/684,915, 2003 - Google Patents

... CELLS switching module 51 TRANS. CELLS *••4 HyperTransport/ **SPI-4**/PCI/etc. ... Rx MAC 66 Tx MAC 68 (Agent B) (Agent B) HyperTransport/ **SPI-4**/PCI/etc. ...

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Controlling access to sections of instructions

DF Hooper, A Kumar - US Patent App. 10/445,168, 2003 - Google Patents

... The processor 500 can also feature an interface 502 (eg, a **System Packet Interface** Level 4 (**SPI-4**) interface) that enables to the processor 500 to communicate ...

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Tired of Messy EMI Solutions? Gore is the Indispensable Choice!

HS Effectiveness, NC Required - IEEE Communications Magazine, 2001 - [ieeexplore.ieee.org](#)

Page 1 Tired of Messy EMI Solutions? Gore is the Indispensable Choice!

GORE-SHIELD0 EM! Gaskets are Customized, Pre-Formed Materials ...

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Designing and testing the interconnection of addressable devices of integrated circuits

RNC Broberg, TE Faber, GS Delp, PG Reuland, DJ ... - US Patent App. 10/465,186, 2003 - Google Patents

Page 1. US 20040261050A1 (19) United States (12) Patent Application Publication

(io> Pub. NO.: US 2004/0261050 AI Broberg, III et al. (43) Pub. Date: Dec. ...

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High data rate stateful protocol processing

FI Osman, SJ Knee - US Patent App. 10/211,434, 2002 - Google Patents

Page 1. US 20040024894A1 (19) United States (12) Patent Application Publication

(io> Pub. NO.: US 2004/0024894 AI Osman et al. (43) Pub. Date: Feb. ...

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Deskew architecture

GR McLeod - US Patent App. 10/284,575, 2002 - Google Patents

... One such bus standard is the **System Packet Interface** Level 4 Phase 2 (**SPI-4** Phase 2) bus standard specification, such as version 2000.088.4 available from the ...

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Network processor having bypass capability

TC Reiner, K Jong, P Terry, N Walls, C Haywood, M ... - US Patent App. 10/374,214, 2003 - Google Patents

Page 1. US 20040165590A1 (19) United States (12) Patent Application Publication

(io> Pub. NO.: US 2004/0165590 AI Reiner et al. (43) Pub. Date: Aug. ...

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Method and apparatus for graphically programming a programmable circuit

SA Davidson, SC Mickelson, GT Sarkinen, SA ... - US Patent App. 10/017,756, 2001 - Google Patents

Page 1. US 20030110464A1 (19) United States (12) Patent Application Publication

(io> Pub. NO.: US 2003/0110464 AI Davidson et al. (43) Pub. Date: Jun. ...

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[PDF] ► Final Report for the 10 to 100 Gigabit/Second Networking Laboratory Directed Research and ...

EL Witzke, LG Pierson, TD Tarman, LB DEAN, PJ ... - 2001., 2001 - [infoserve.sandia.gov](#)

Page 1. SANDIA REPORT SAND2001-1062 Unlimited Release Printed April 2001 Final Report for the 10 to 100 Gigabit/Second Networking Laboratory ...

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"SPI-4" and system-packet-interface

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